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EXAMINER
TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,065	WEHAGE, ERIC R.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim recites "... and storing a test pattern for use with the plurality of states". The disclosure does not discuss storing a test pattern that may be used by the state machine. The examiner cannot determine the structure or location of such a storage device, nor the means by which the state machine would utilize the same, because the disclosure did not provide that information.

2. Claims 2, 8 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim recites, "... no more than four state machines are used by the BIST state machine". The examiner is not sure what this means, because "four states" does not ensure less than five state machines, and this has not been taught in the disclosure.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 8 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites, "... no more than four state machines are used by the BIST state machine". The examiner is not sure what this means, because "four states" does not ensure less than five state machines.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ledford et al., U.S. Patent No. 6760865, in view of Huang et al., U.S. Patent No. 6415403. Ledford et al. teaches method based on an integrated circuit comprising a built-in self test (BIST) state machine (see Title and FIG.2 51), having: a plurality of states to conduct a plurality of tests (column 5 lines 54-63) for a random access memory (column 1 lines 13-51), a command register coupled to the plurality of states (FIG.2 58and column 2 lines 29-60) and storing a test pattern for use with the plurality of states (FIG.3 74); and an address counter coupled to the plurality of states to

determine a test location in the RAM (FIG.3 76). Each state of state machine 51 controls the operations of state machine 70 (nested states), and therefore all functions of 70 are executed in any state of 51 (example: column 5 lines 54-63). But Ledford et al. fails to specifically teach that each state is capable of performing a null operation, a write operation, a read operation, and a read/write operation, by name. But in an analogous art, Huang et al. discusses the operations executed by name in column 6 lines 14-58 and FIG.4. In column 2 lines 16-40, Huang et al. states that the BIST state machine of the invention offers a less complex means of testing embedded memories of all kinds. One with ordinary skill in the art at the time of the invention, motivated as suggested above, would find it obvious to combine the Huang et al. state machine with the specific operations listed above, into the state machine 70 of Ledford et al., in order to fully utilize the BIST of Ledford et al.

5. Claims 2, 3, 5, 6, 8-10, 12-14, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ledford et al., U.S. Patent No. 6760865, in view of Huang et al., U.S. Patent No. 6415403 as applied to Claim 1, and further in view of Barry et al., U.S. Patent No. 5825785.

As per Claims 2, 8 and 17:

Ledford et al. and Huang et al. fail to further teach the method/integrated circuit of claim 1, 7 or 16, wherein the plurality of states consists of only four states to ensure that no more than four state machines are used by the BIST state machine for a test. But in the analogous art of Barry et al., a state machine consisting of four states is featured (column 5 lines 35-36). And in column 2 lines 16-28, a flexible BIST design is proposed

which can be in variably designed hardware. One with ordinary skill in the art at the time of the invention, motivated as suggested, would combine the hardware of Barry et al. to the teachings of Ledford et al. and Huang et al. in order to have more flexibility in manufacturing differing integrated circuits.

As per Claims 3, 9 and 18:

Barry et al. further teaches the method/integrated circuit of claim 1, 7 or 16, wherein one of the plurality of states is an idle state (column 5 lines 35-36), but does not teach; to which the BIST state machine returns after a final address or an error is detected. But Huang et al., in FIG.4 does teach this feature. And in view of the motivation stated previously, the claims are rejected.

As per Claims 5, 10 and 19:

Ledford et al. further teaches the method/integrated circuit of claim 1, 7 or 16, comprising an additional counter to cause a state to repeat an assigned operation (FIG.2 54 and column 3 lines 50-67 and column 4 lines 1-42). And in view of the motivation stated previously, the claims are rejected.

As per Claims 6, 12 and 13:

Barry et al. further teaches the method/integrated circuit of claim 1 or7, wherein the address counter is incremented/decremented whenever a first state transitions to itself in a single state chain or to a second state positioned prior to the first state in a multiple state chain (column 5 lines 30-65 and FIG.3). And in view of the motivation stated previously, the claims are rejected.

As per Claim 14:

Ledford et al. further teaches the method of claim 7, further comprising signaling to the BIST state machine to read from both a static address and the test location (column 5 lines 8-53). And in view of the motivation stated previously, the claims are rejected.

6. Claims 4, 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ledford et al., U.S. Patent No. 6760865, in view of Huang et al., U.S. Patent No. 6415403 as applied to Claim 1, 7 or 16 and further in view of Agrawal et al., "An Architecture for Synthesis of Testable Finite State Machines". The method/integrated circuit of claim 1, 7 or 16, wherein one state of the plurality of states assigned to perform the null operation is skipped during transitioning between the plurality of states is not taught by Ledford et al. and Huang et al. But, in a four state machine as described by Agrawal et al., it is shown to be common practice in the art to skip or select states in a state machine as is shown in FIG.5. Agrawal et al. in column 2 of page 612 states that the ideas set forth elevate the design for testability into the synthesis procedure. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to skip states in a state machine, and in particular, one such as used by Ledford et al. and Huang et al.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ledford et al., U.S. Patent No. 6760865, in view of Huang et al., U.S. Patent No. 6415403 as applied to Claim 7, and further in view of Phan, U.S. Patent No. 6425103. The references cited for Claim 7 do not teach the method of claim 7, further comprising inverting data based on a least significant address bit. But Phan, in the Abstract does

teach this feature. And column 2 lines 15-67 and column 3 lines 1-15, a more effective way to generate addresses for the moving inversion test method is disclosed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the teachings of Phan to the circuit such as used by Ledford et al. and Huang et al. for more efficient execution of the moving inversion method.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings

Examiner
Art Unit 2133

jpt

GUY J. LAMARRE
PRIMARY EXAMINER